JOINT INVENTORS

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Richard Zimmermann

APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that we, Sung-Kwon LEE, a citizen of the Republic of Korea, residing at San 136-1, Ami-Ri, Bubal-Eub, Ichon-Shi, Kyoungki-Do 467-860, in the Republic of Korea, and Sang-IK KIM a citizen of the Republic of Korea, residing at San 136-1, Ami-Ri, Bubal-Eub, Ichon-Shi, Kyoungki-Do 467-860, in the Republic of Korea, have invented a new and useful METHOD FOR MANUFACTURING MULTI-LEVEL INTERCONNECTIONS WITH DUAL DAMASCENE PROCESS, of which the following is a specification.

METHOD FOR MANUFACTURING MULTI-LEVEL INTERCONNECTIONS WITH DUAL DAMASCENE PROCESS

BACKGROUND

Technical Field

A method for manufacturing a semiconductor device is disclosed which includes forming multi-level interconnection lines with a dual damascene process.

Description of the Related Art

Recently, with increased integration of a semiconductor device, a limit results in connection with decreasing the line width using a photolithography process, which is used in semiconductor manufacturing processes. To solve the above-mentioned problem, a damascene process has been used.

Generally, a trench is formed by etching an insulating layer, and a interconnection line is formed in the trench by a self-align dual damascene process.

In the self-align dual damascene process, a via connecting the lower and upper interconnection lines is aligned at a bottom of the trench. That is, in the self-align dual damascene process, an insulating layer is selectively etched with the photolithography process to form a trench exposing a via at the bottom thereof, and a conductive layer is formed with W, Al or Cu to fill the trench. After that, the conductive layer outside of the trench, namely a portion of the conductive layer, which is not necessarily needed, is removed by an etching or a chemical mechanical polishing (CMP) to form a interconnection line in the trench.

The above-mentioned self-align dual damascene process is mainly used for forming a bit line, a word line and a metal interconnection line of a dynamic random access memory (DRAM). Specially, by the self-align dual damascene process for forming the trench, a via hole used to form a via connecting upper and lower interconnection lines, may be formed simultaneously. By the self-align dual damascene process, a height difference due to interconnection lines may not be generated, since the via and interconnection lines are buried in interlayer insulating layers.

Figs. 1A to 1D are cross-sectional views illustrating a conventional method for forming a multi-level metal interconnection line according to a conventional self-align dual damascene process.

Referring to Fig. 1A, interlayer insulating layers 12 and 13 and an etching stop layer 14 are formed on a semiconductor substrate 11. After that, the etching stop layer 14 and the interlayer insulating layer 13 are selectively etched to expose an area where a first metal interconnection line is to be formed.

Subsequently, a metal layer is deposited on the exposed area and selectively removed to form a metal interconnection line 15 in the etching stop layer 14 and the interlayer insulating layer 13.

Referring to Fig. 1B, a third interlayer insulating layer 16 is formed on the etching stop layer 14 and the metal interconnection line 15. An etching stop layer 17 and a fourth interlayer insulating layer 18 are successively formed on the third interlayer insulating layer 16, and a photoresist layer (not shown) is formed on the fourth interlayer insulating layer 18, then a via

hole mask (not shown) is formed by exposing and developing the photoresist layer.

Subsequently, the fourth interlayer insulating layer 18, the etching stop layer 17 and the third insulating layer 16 are etched using the via hole mask to form a via hole 19, which exposes a predetermined surface of the metal interconnection line 15.

Then, after removing the via hole mask, a photoresist layer is formed on the fourth interlayer insulating layer 18 in which the via hole 19 is formed and a trench mask 20, exposing a larger area than the via hole 19, is formed by exposing and developing the photoresist layer.

Referring to Fig. 1C, a trench 21 is formed by etching the fourth interlayer insulating layer 18 using the trench mask 20. When the trench 21 is formed, the etching is stopped at the etching stop layer 17.

Referring to Fig. 1D, after removing the trench mask 20, a metal layer is deposited on the resulting structure, then an etch back or a chemical mechanical polishing (CMP) is carried out until the surface of the fourth interlayer insulating layer 18 is exposed, and thereby to form a metal interconnection line 22 in the trench 20. When the metal interconnection line 22 is formed, a via 22a connected to the metal interconnection line 15 is formed in the via hole.

As shown in Fig. 2A, after forming the trench by etching the fourth interlayer insulating layer 18, the etching stop layer 17 is left except the via hole region. The etching stop layer 17 is usually formed with the nitride layer having a high capacitance value, in this case, a problem of capacitance increase is occurred due to the remaining etching stop layer 17.

Also, as shown in Fig. 2B, when the thicknesses of insulating layers are increased, the etch profile on the corner (A) of the trench may be distorted due to the low etch selectivity between the insulating layers formed with the oxide layers and the etching stop layer formed with the nitride layer.

SUMMARY OF THE DISCLOSURE

A method for forming multi-level interconnection lines using a dual damascene process is disclosed. With the dual damascene process, it is easy to control distortion of a profile on a corner of a trench, and to prevent capacitance value from increasing due to a remaining etching stop layer.

A disclosed method for manufacturing multi-level interconnection lines of a semiconductor device comprises: forming a first interconnection line on a semiconductor substrate; forming a first interlayer insulating layer on the first interconnection line; forming a first etching stop layer on the first interlayer insulating layer; forming a via hole exposing the first interconnection line by selectively etching the first etching stop layer and the first interlayer insulating layer; forming etching stop patterns around an inlet of the via hole by selectively etching the first etching stop layer; forming a second interlayer insulating layer on the etching stop pattern and the first interlayer insulating layer; forming a trench by selectively etching the second interlayer insulating layer; and forming a conductive layer in the trench and in the via hole.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects of the disclosed methods will become apparent from the following description with reference to the accompanying drawings, aherein:

Figs. 1A to 1D are cross-sectional views illustrating a conventional method of manufacturing metal interconnection lines using a dual damascene process;

Fig. 2A is a perspective view illustrating a remaining etching stop layer after etching a trench in accordance with the conventional method;

Fig. 2B is a perspective view illustrating a profile distortion at a corner of a trench formed in accordance with the conventional method; and

Figs. 3A to 3E are cross-sectional views illustrating a method of manufacturing metal interconnection lines using a dual damascene process in accordance with the disclosure.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMODIMENTS

A method of manufacturing multi-level interconnects using a dual damascene process will be described in detail referring to the accompanying drawings.

Figs. 3A to 3E are cross-sectional views illustrating a method of manufacturing metal interconnection lines using a dual damascene process.

Referring to Fig. 3A, in a method of manufacturing multi-level metal interconnection lines, interlayer insulating layers 32 and 33 and an etching stop layer 34 are formed on a semiconductor substrate 31. After that, the etching stop layer 34 and the interlayer insulating layer 33 are selectively etched to expose a part where a metal interconnection line is to be formed.

Subsequently, a metal layer is deposited on the exposed part and selectively removed to form a metal interconnection line 35 in the etching stop layer 34 and the interlayer insulating layer 33.

Referring to Fig. 3B, a third interlayer insulating layer 36 is formed on the etching stop layer 34 and the metal interconnection line 35. An etching stop layer 37 is formed on the third interlayer insulating layer 36. Thereafter, a photoresist layer is coated on the etching stop layer 37 and exposed and developed to form a via hole mask 38.

The etching stop layers 34 and 37 are formed with any one selected from the group consisting of a nitride layer formed by a plasma enhanced chemical vapor deposition(hereinafter referred as PECVD), a SiON layer, a Ta_2O_5 layer, a ZnO_2 layer, a ZrO_2 layer, a ZnO layer, a HfO layer and an Al_2O_3 layer, at a thickness ranging from about 200 Å to about 3000 Å. Also, the interlayer insulating layers 32, 33 and 36 are formed with any one selected from the group consisting of a spin on glass(SOG) layer, an oxide layer formed with the PECVD method, a tetra-ethyl-ortho-silicate(TEOS) layer, an oxide layer formed with high density plasma(hereinafter referred as HDP), and other insulating layers having a low dielectric constant, at a thickness ranging from about 3000 Å to about 30000 Å.

Next, the etching stop layer 37 and the third interlayer insulating layer 36 are etched using the via hole mask 38 to form a via hole 39, which exposes a predetermined portion of the metal interconnection line 35.

Referring to Fig. 3C, after removing the via hole mask 38, another photoresist layer is coated on a

resulting structure and is exposed and developed to form a photoresist pattern 40 covering the etching stop layer 37 near the via hole 39. The width d_1 of the photoresist pattern 40 is larger than that of a trench to be formed later, as much as 0.2 μm to 1.0 μm, which is a minimum size of a part needed in an etching process for forming a trench.

Successively, the etching stop layer 37 is etched using the photoresist pattern as an etch mask to form an etching stop pattern 37a around the via hole, that is the etching stop pattern 37a is left at parts where an etching stop layer is needed to form a trench. Therefore, even if the etching stop pattern 37a is formed with a layer having high dielectric constant, such as a nitrogen layer, the capacitance increase due to the etching stop pattern 37a may be reduced.

Referring to Fig. 3D, the etching stop pattern 37a is exposed by removing the photoresist pattern 40, and a fourth interlayer insulating layer 41 is formed on a resulting structure.

The fourth interlayer insulating layer 41 is formed with any one selected from the group consisting of a HDP-USG layer, an undoped silicate layer deposited by the HDP, and an oxide layer deposited by the PECVD method or low pressure chemical vapor deposition method(LPCVD), and the fourth interlayer insulating layer 41 is formed at a thickness ranging from about 2000 Å to about 30000 Å, in order to form a void (B) is formed in the via hole 39.

After forming the fourth interlayer insulating layer 41, a photoresist layer is coated on the fourth interlayer insulating layer 41, and a trench mask 42 is formed by exposing and developing the photoresist layer. At this time, the width d_2 of the trench defined by the

trench mask 42 is narrower than that of the via hole, that is spacing between the etching stop layer patterns 37a.

Referring to Fig. 3E, a trench is formed by etching the fourth interlayer insulating layer 41 using the trench mask 42 as an etch mask. At this time, the etching is stopped at the etching stop layer patterns 37a. The etching target may be decreased as much as the size of the void (B) generated in the formation of the fourth insulating layer 41.

After removing the trench mask 42, a metal layer is deposited on the resulting structure, and an etch back or a chemical mechanical polishing (CMP) is performed until the surface of the fourth interlayer insulating layer 36 is exposed to form a metal interconnection line 43 in the trench, and at the same time a via 43a, connecting the metal interconnection line 43 to the metal interconnection line 35, is formed in the via hole 39.

The metal interconnection lines 35 and 43 and the via 43a may be formed with any one selected from the group consisting of Al, Cu, Au, Ag and Cr. The metal layers are deposited at a thickness ranging from about 2000 Å to about 30000 Å by using any one selected the group consisting of a chemical vapor deposition (CVD), an electroless deposition and a physical vapor deposition (PVD).

Meanwhile, before forming the metal interconnection line 43, a diffusion barrier layer may be formed at a thickness ranging from about 1000 Å to about 5000 Å. The diffusion barrier layer is formed with any one selected from the group consisting of a TiN layer, a Ti layer, a W layer, a WN layer and a TiW layer is deposited

In the above-mentioned embodiments the disclosed method is for forming a multi-layer metal interconnection line. However, the disclosed method may be adapted in a method for forming a word line, a bit line and a contact, which have a dual damascene structure.

The disclosed method may prevent increasing of a capacitance value by remaining an etching stop layer for forming trench and decreasing etching target by etching a interlayer insulating layer where a void is already formed, so that a margin of a trench etching process may be maximized.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

Advanced Semiconductor